Timing the Trigger:
Clock Signal Distribution in the CMS Level 1 Trigger System

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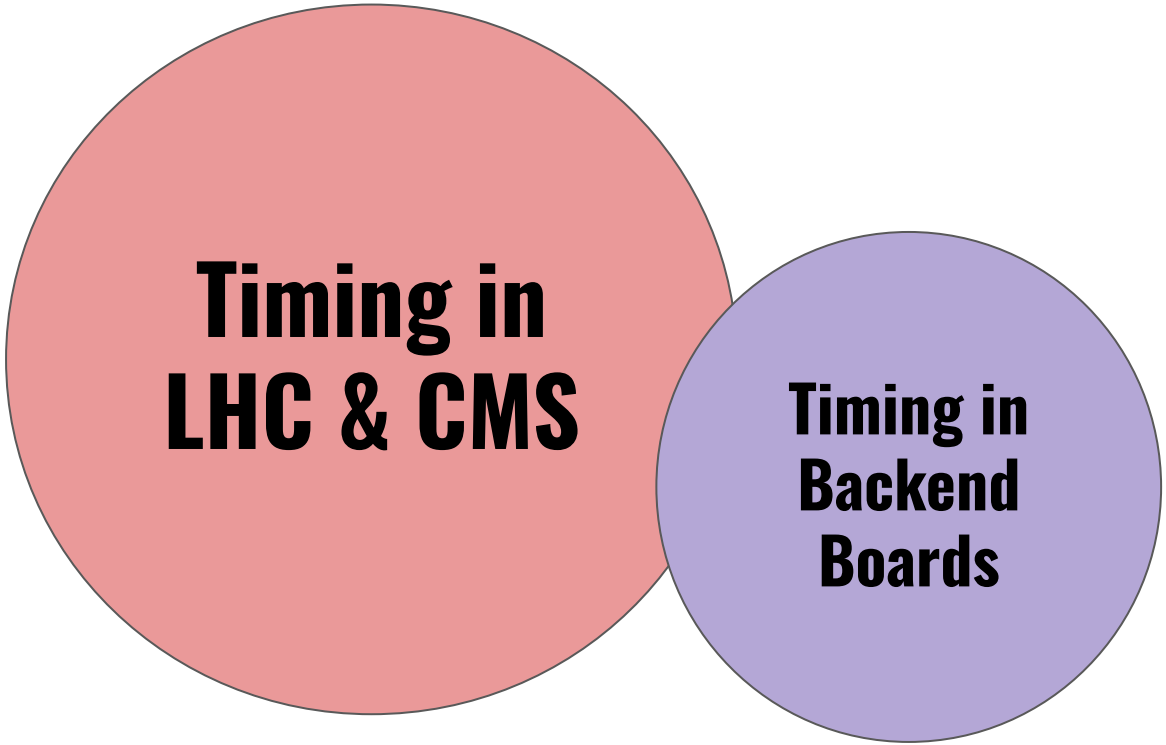
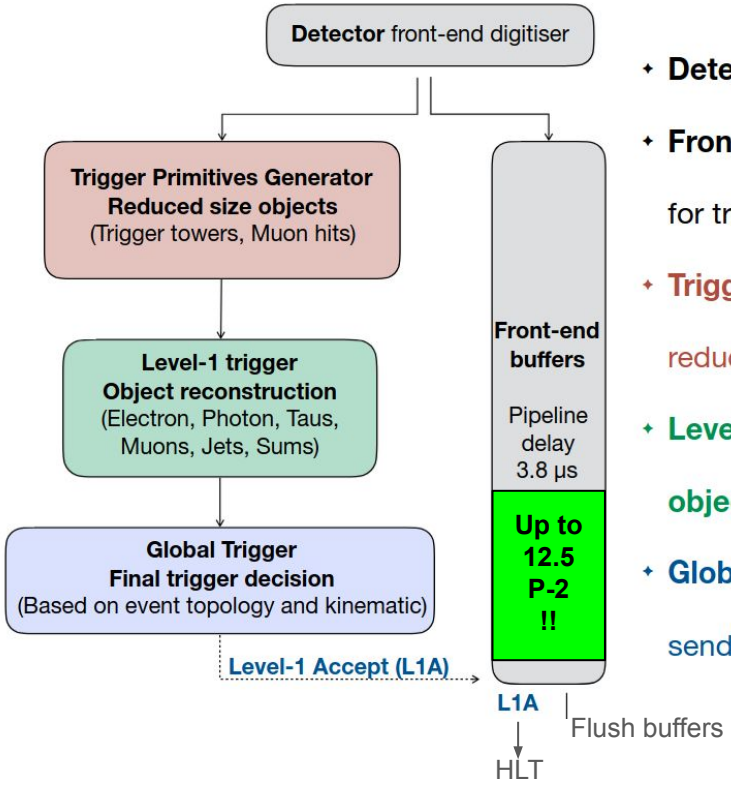
Summary

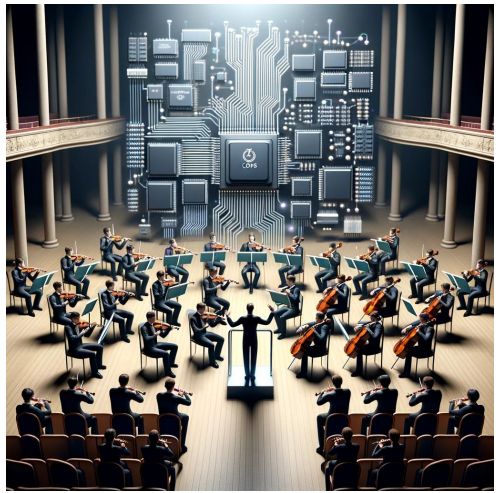


How does a trigger system work ?



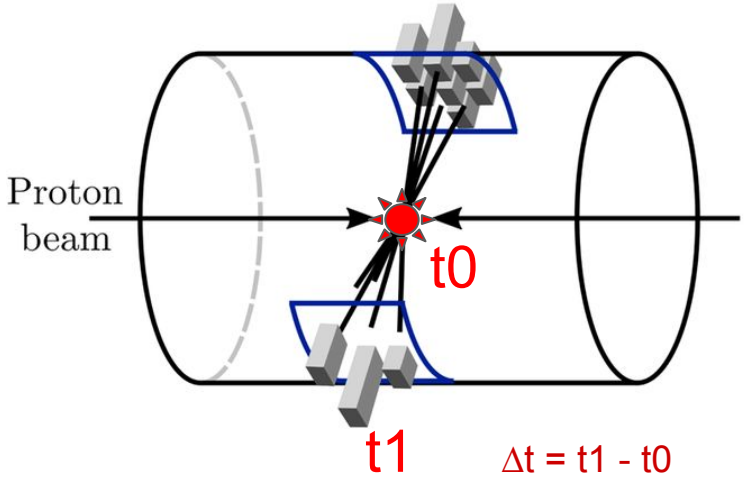
- **Detector** signals duplicated at front-end
- **Front-end buffers** store full event waiting for trigger decision
- **Trigger primitive generators** produce reduced size objects
- **Level-1 processors** reconstruct **physics objects** from trigger primitives
- **Global trigger** takes **final decision** and sends it to buffers for **disk storage or flush**

How do we synchronize all these events?



Timing in LHC

¿How do we measure the timing?



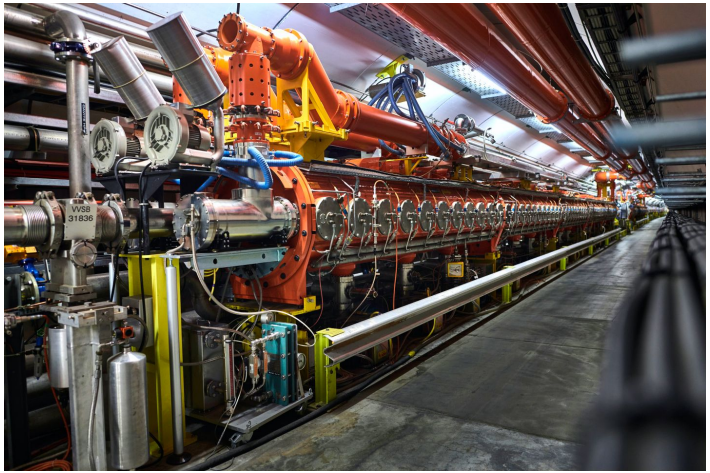
- **t0** marks the beginning of the measurement, collision. Provided by the accelerator.
- **t1** marks the arrival of the particle to the detector using TDCs. Analog sensor to timing information conversion (LYSO crystals, SiPMs, LGAD sensors…)

Timing in LHC - Tzero

- Bunch of particles are arranged by the **RF cavities** that are tuned to operate at 400.788 MHz.
- A bunch spacing of approximately **25ns** is achieved in these cavities.
- These neatly spaced bunches then collide at the interaction points of the LHC.
- The readout of the detectors is and should be synchronized to this clock.

Bunch crossing

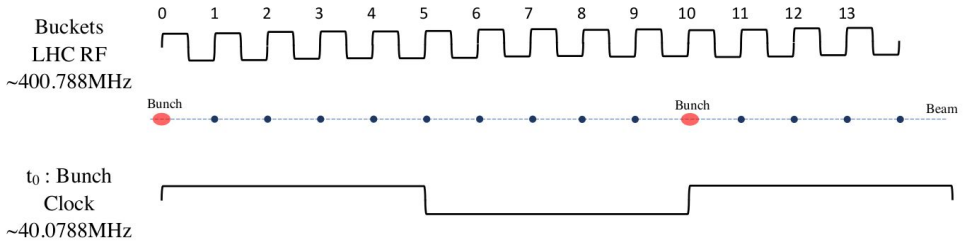
- This the **t0 of the collision** - hence the start of the timing measurement.



Nº: 8x

T: 4.5 K

V: 2 MV

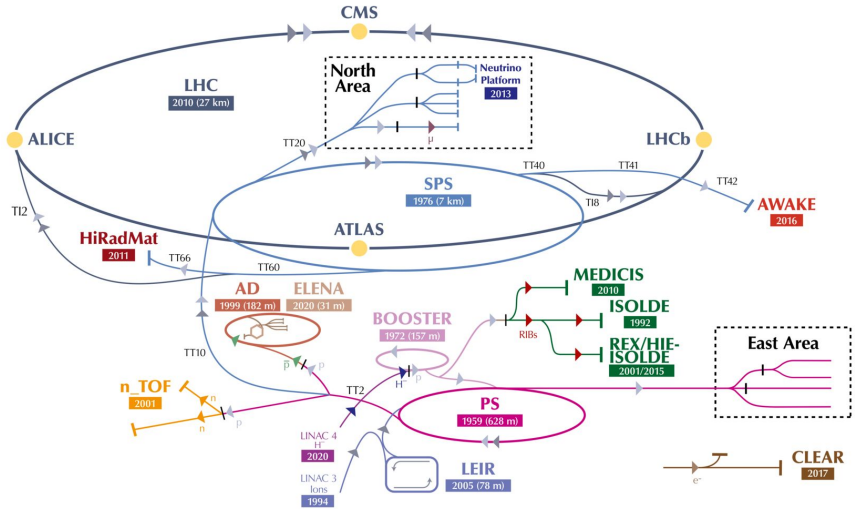


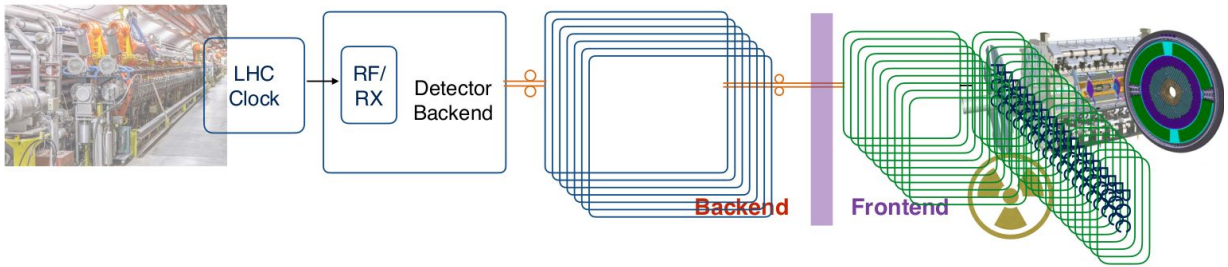
Timing in LHC - Timing distribution to the detectors

Now we have the **t0.**

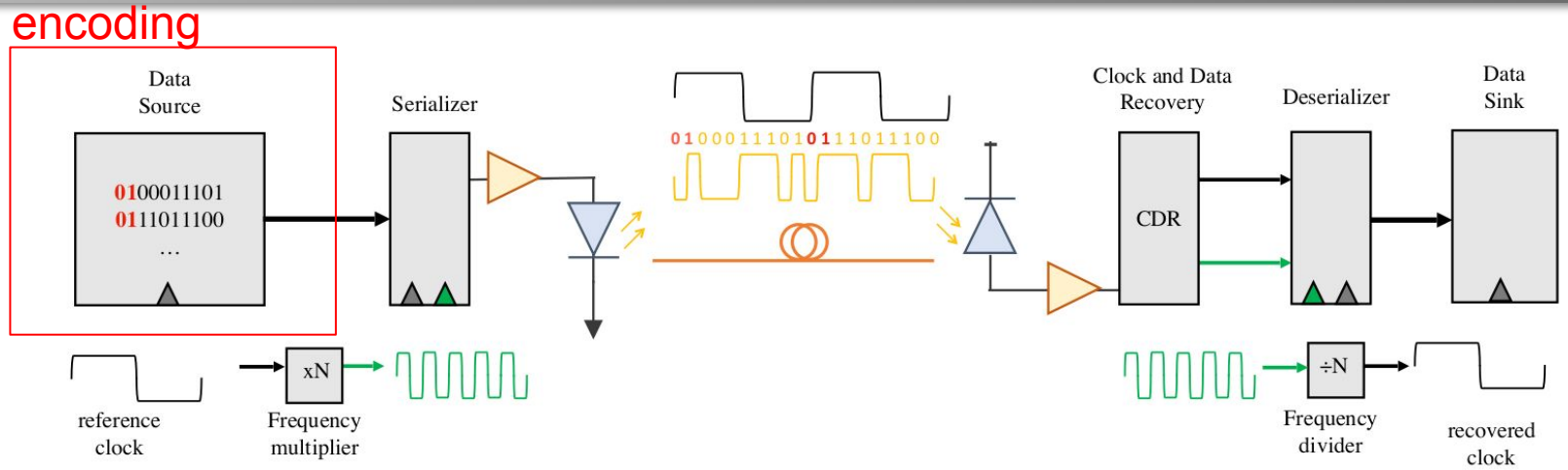
- **How do we distribute it to the detectors?**
  - There may be multiple connection points, opto-electrical conversions, KMs to reach the detector and some hundred meters to be **distributed over tens of thousands of communication links** within a detector!

-





Timing in LHC - Embedded clock



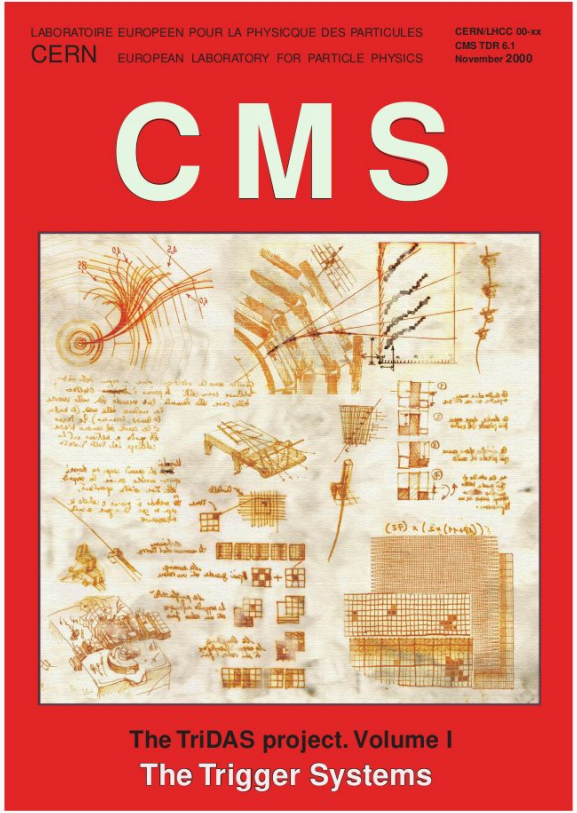
- Rather than distributing a square wave clock, the alignment data is transmitted encoded in the data (more efficient).
- The receiver extracts the alignment information by checking the header bits and reconstructs the clock.
- This allow us to transmit the clock and data in the same link cable.

Manchester encoding, 8b/10b, NRZ …

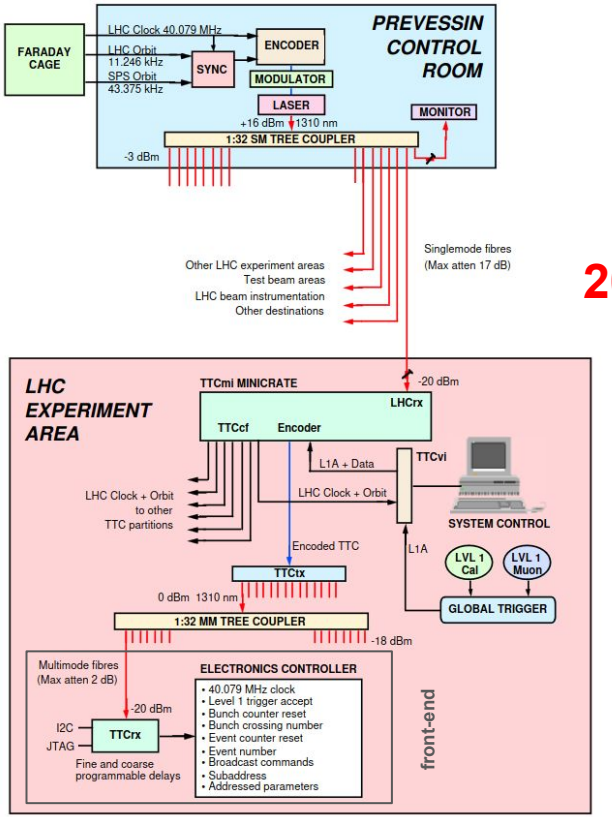
Timing in LHC - Trigger Control & Distribution System

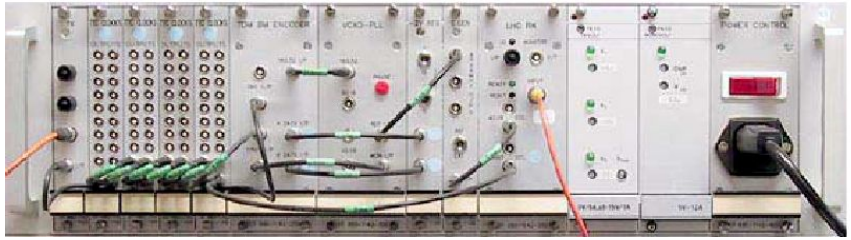
In the original CMS design trigger control, trigger distribution, and synchronisation were handled by three separate systems:

- **TTC**: **T**rigger, **T**iming and **C**ontrol.
  - Optically transmit the LHC clock and fast commands to detector front-ends.
- **TTS**: **T**rigger **T**hrottling **S**ystem.
  - Gather status information from the readout electronics.
- **TCS**: **T**rigger **C**ontrol **S**ystem.
  - Control the delivery of L1 Trigger Accept (L1A) signals based upon the status of the readout electronics and DAQ system.



Timing in LHC - Trigger Timing and Control (TTC)

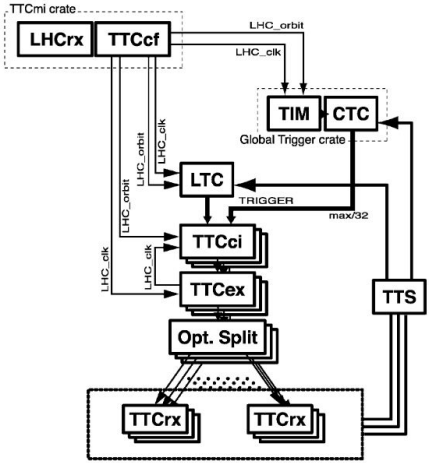




TTCmi minicrate

2009 to 2012

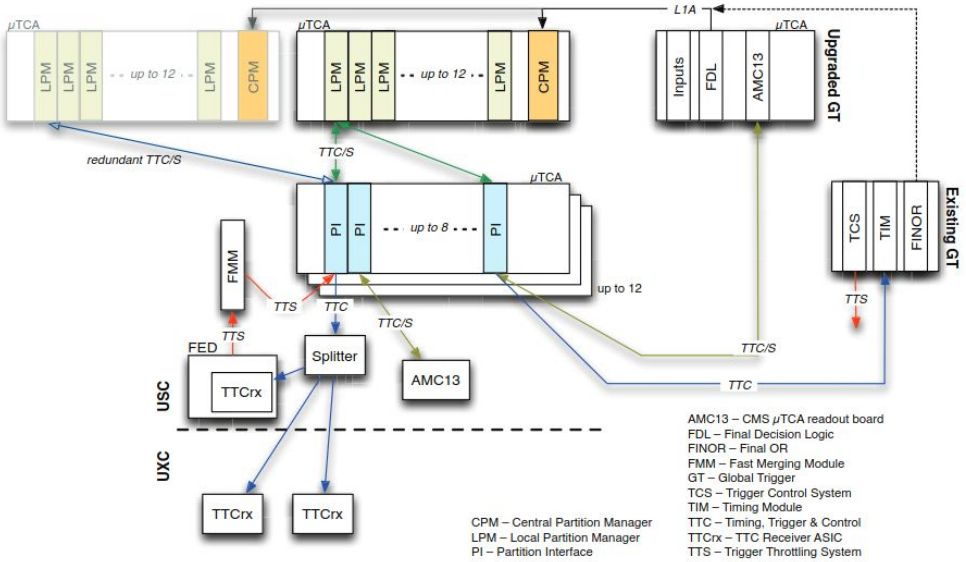
- The LHC Clock and Orbit signals are distributed from the Prevessin Control Room to the LHC experiments through single-mode optical fibers via the TTC Machine Interface (TTCmi) crate.
- High-power, all-glass passive optical networks.
- The trigger system is interfaced with the TTC through the TTC-VMEbus TTCvi (TTCci in CMS).
- At each front-end destination, a special timing receiver ASIC (TTCrx) delivers all the signals required by the electronics controllers.



Timing in LHC - TCDS

Trigger and Timing Control and Distribution System

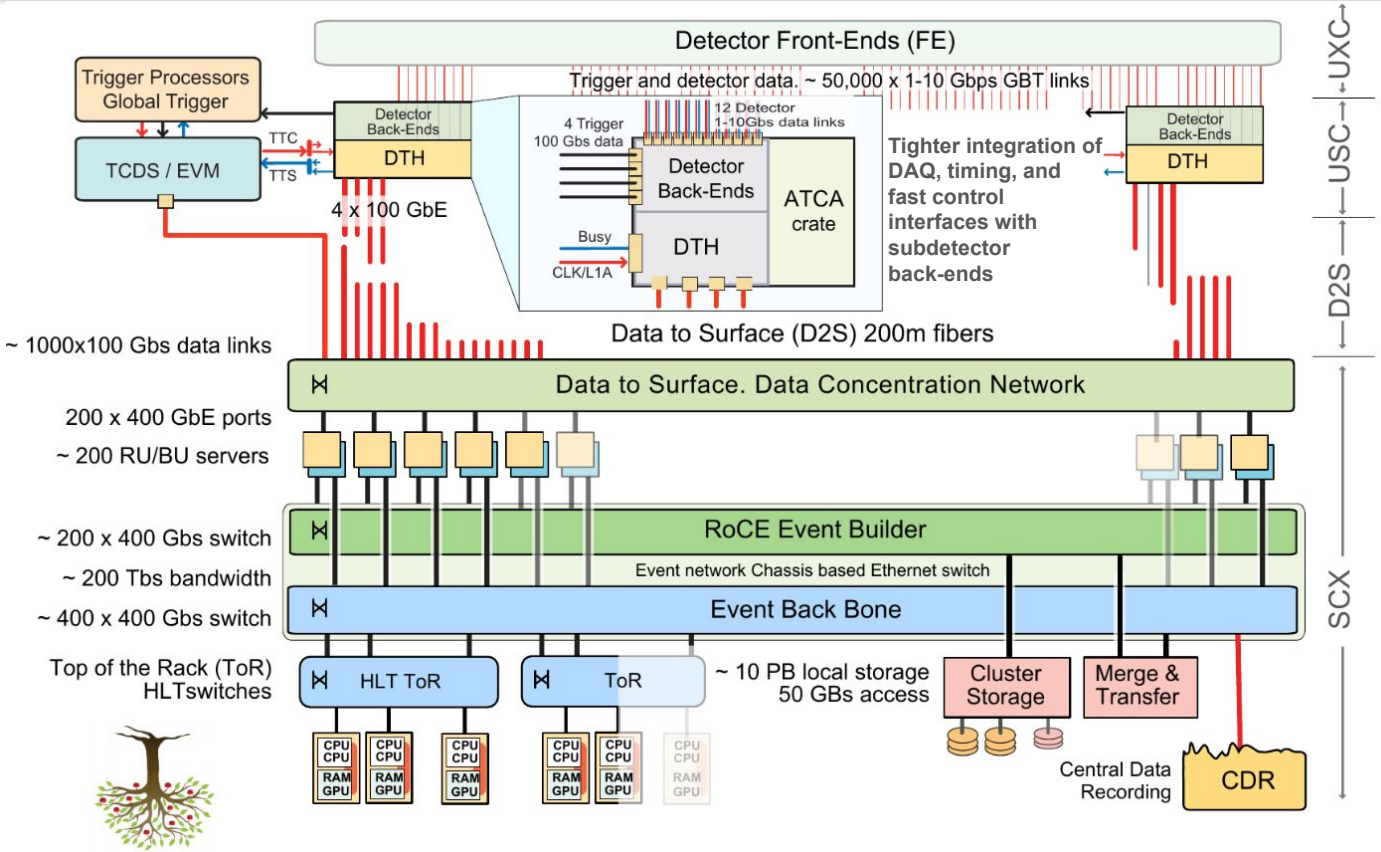
- TTC, TTS, and TCS harmonized into a single system.
- Normalization of functionalities and architecture.
- Massive cleanup.



2015

- MicroTCA based.
- 12-slot crate distributes clock and commands from CPM into LPMs, and aggregates TTS the other way.
- 40MHz | 160Mb/s

Timing in LHC - TCDS2



Phase-I -> **TCDS**

Phase-II -> **TCDS2**

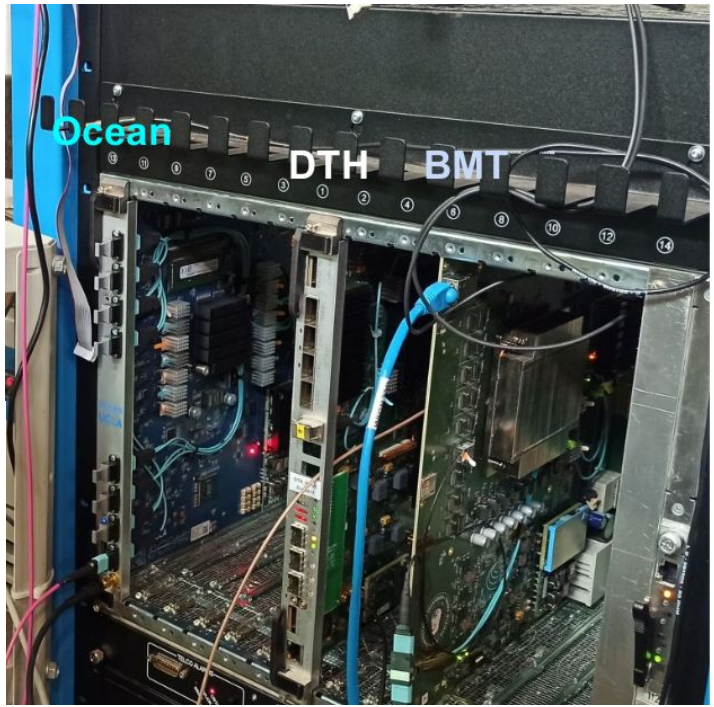
All detectors will be either completely new or significantly upgraded → no backward compatibility required.

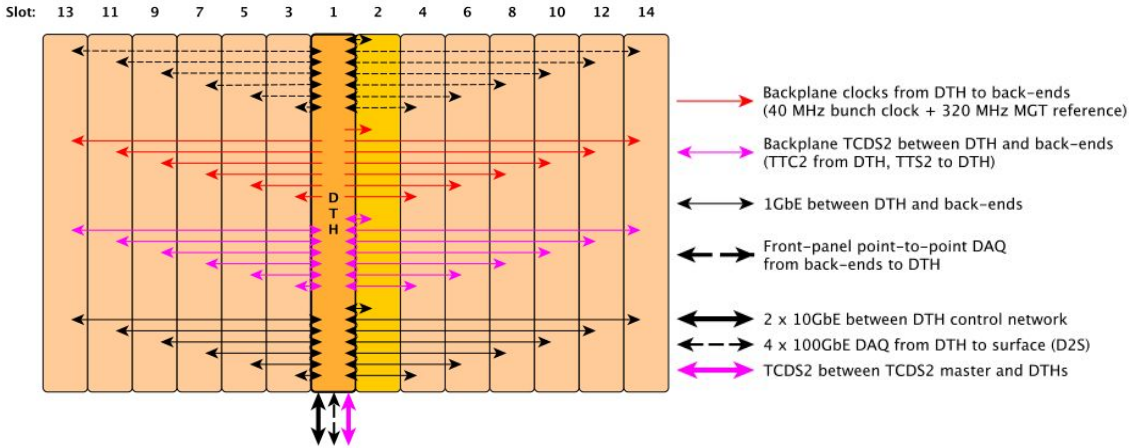
Addition of timing detectors introduces tight clock distribution requirements.

Timing in LHC - TCDS2 distribution, DAQ and Timing Hub (DTH)

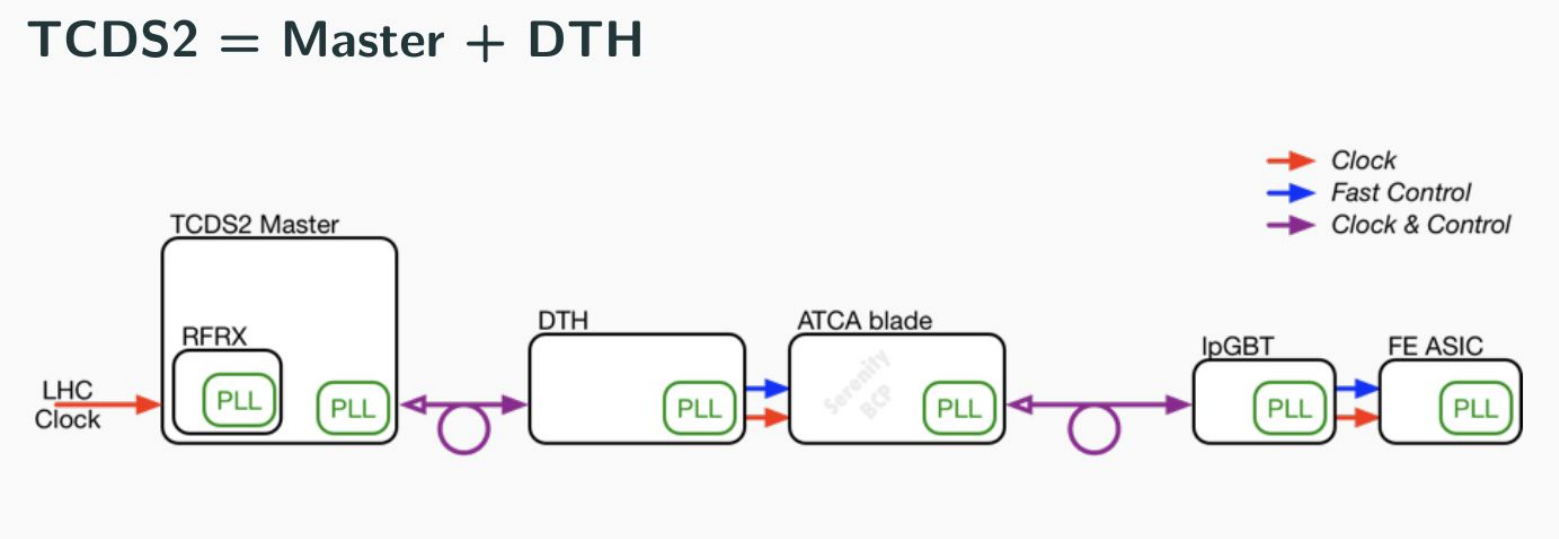
Lives between the synchronous world of L1 trigger and detectors and the asynchronous DAQ world.

- Distributes clock signals, synchronization commands, L1 trigger, and slow control from central systems to back-ends.
- Receives event fragments from back-ends, concentrates and buffers these, and transmits them to the data-to-surface network.





TCDS2 example



- The DTH will drive single-crate test/commissioning systems.
- The TCDS2 master will drive multi-crate systems, and synchronise to the LHC.

Level-1 Trigger Processor boards

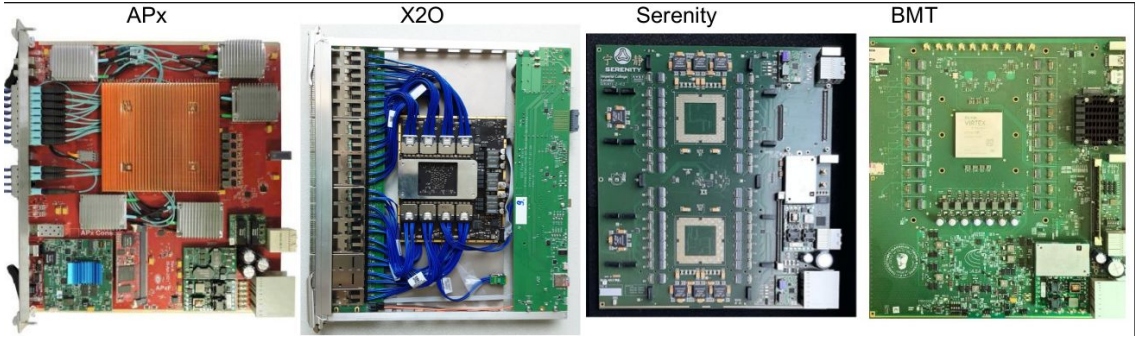
- Based on powerful FPGAs produced by Xilinx.
- Large Input/Output bandwidth using multiple Optical Fibers.
- Parallel data processing by Trigger Algorithms.

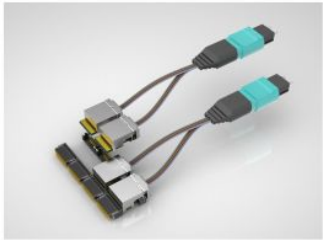
Phase-2 Processors utilize Ultrascale Plus FPGA family:

- Optical module with latest QSFP and QSFP-DD (double-density) optics.
- Samtec Firefly.

Both designed to follow the 25 Gigabit Ethernet standard line rate

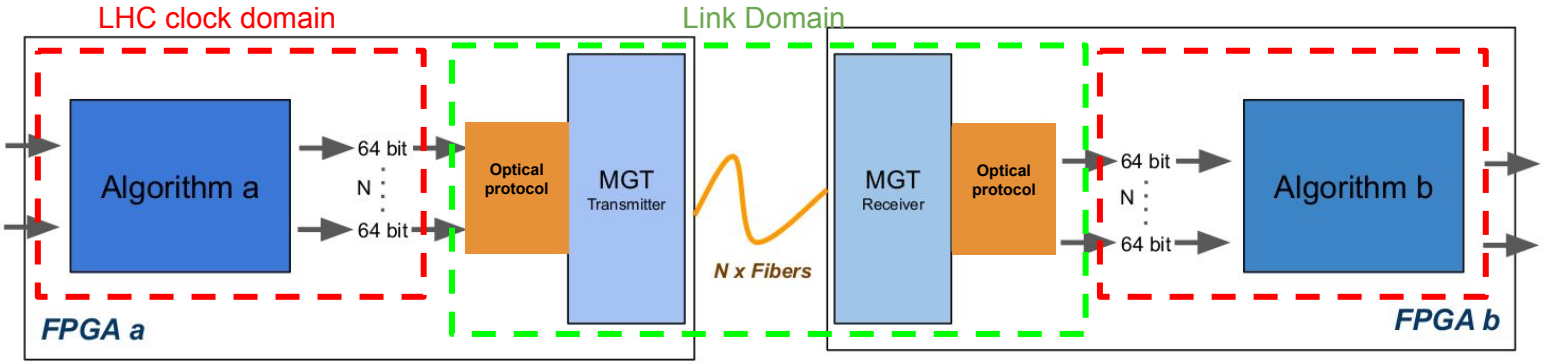
- **25.78125 Gb/s**



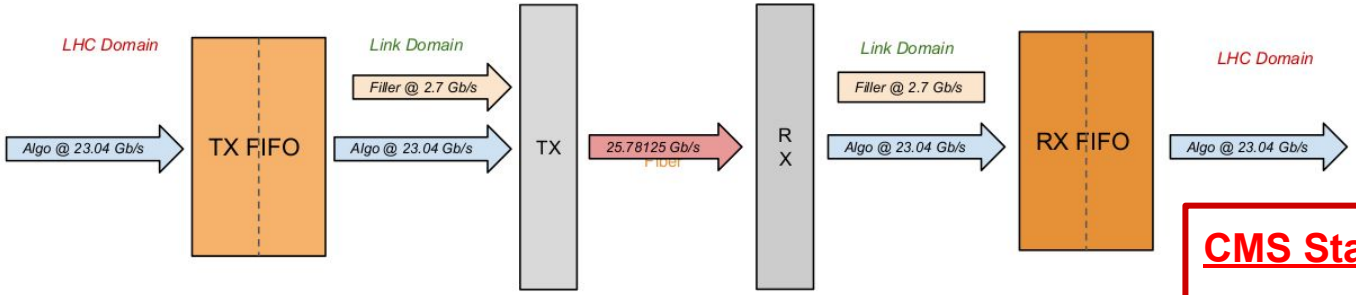


Algorithm Clock vs Link Clock

- CMS systems must be synchronous with the LHC Clock - 40 MHz.
  - Subsystems must “be aware” of which Buch Crossing data they process
  - Algorithm clock domain must be multiple of the LHC clock.
  - To transmit and receive data two Algorithm blocks must utilize the same Optical Protocol.

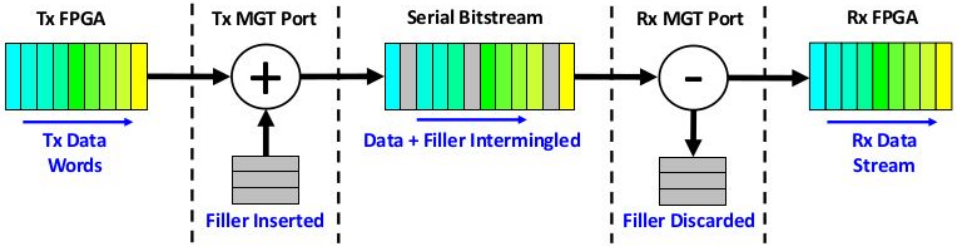


Asynchronous data architecture - Protocols



At **25.78125** Gbps
- Link Domain: **390.6** MHz
- LHC Domain: **360** MHz
- LHC Bandwidth: **23.04** Gbps
- Filler Bandwidth: **2.74125** Gbps

- Utilize FIFOs to handle Clock Domain differences.
- Tx write CD lower than read Rx.
- Filler bandwidth is created when fifo is empty.

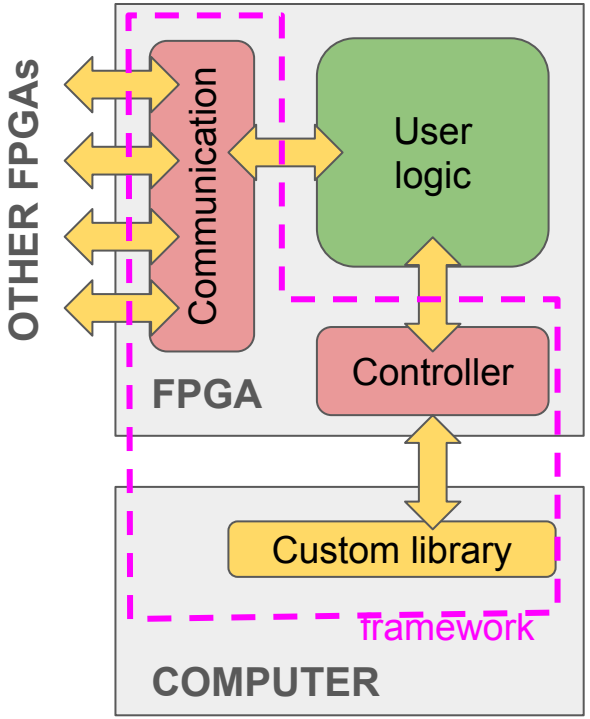


CMS Standard Protocol (CSP)

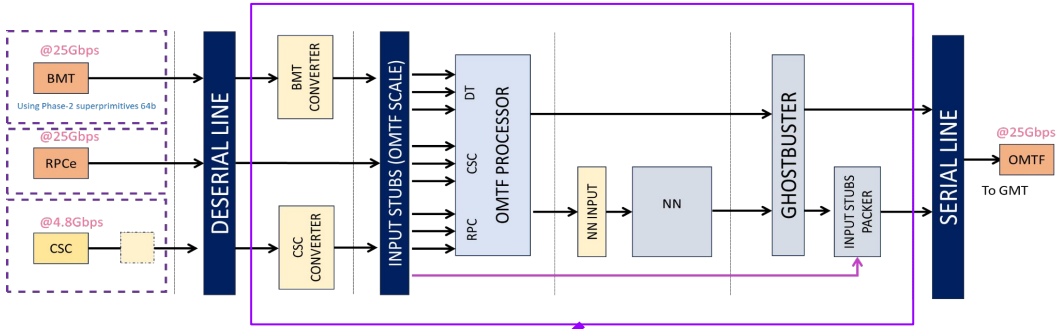
- Serial Data Rate: **24.17 Gbps** (from LHC, 9 data words/Bx, 67-bit word).
- Bandwidth is divided into two categories:
  - "Data" – LHC synchronous physics payload
  - "Filler" – excess bandwidth needed to meet the physical line rate
- Multiple reliability mechanisms.
  - Critical-Field Error Correction
  - CRC16 protection
  - Index Correction
  - Link ID Words

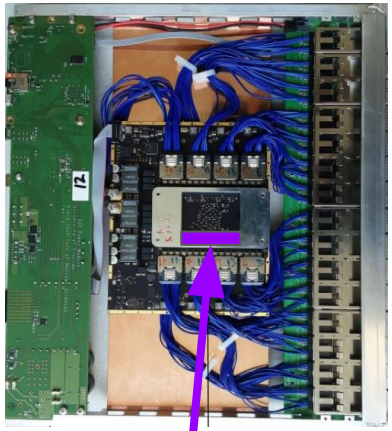
Frameworks

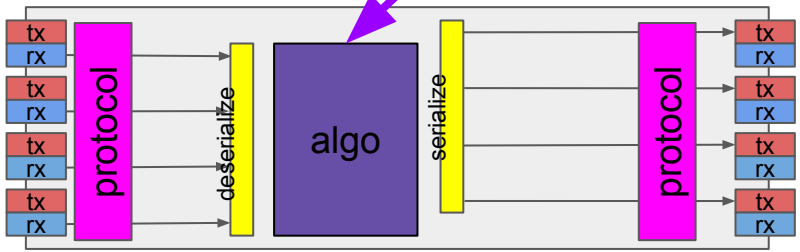
- **Purpose-Driven Design**: Dedicated FPGA frameworks specifically tailored for High-Speed Serial Communications and LHC clock data recovery.
- **Modular Architecture**: Encapsulates all necessary modules including encoding, decoding, error checking, and protocol management.
- **LHC Clock Recovery**: Specialized modules for handling LHC clock synchronization, critical for data alignment across multiple sensors.
- **Abstraction Layer**: Simplifies user interaction by abstracting complex protocols and hardware details, making the frameworks accessible to non-specialists.
- **Enhanced Usability**: Allows easy implementation of custom algorithm modules and adaptations to evolving research needs.
- **Data Management**: Facilitates data injection for testing and efficient output reading for real-time analysis and algorithm refinement.
- **Flexibility and Scalability**: Supports rapid prototyping and scalability in response to changing experimental requirements.

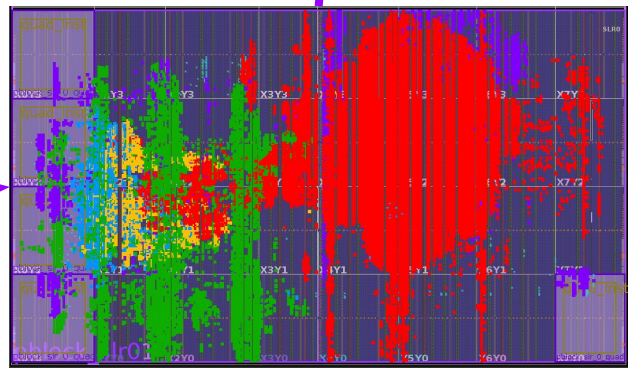


Example of an algorithm integration





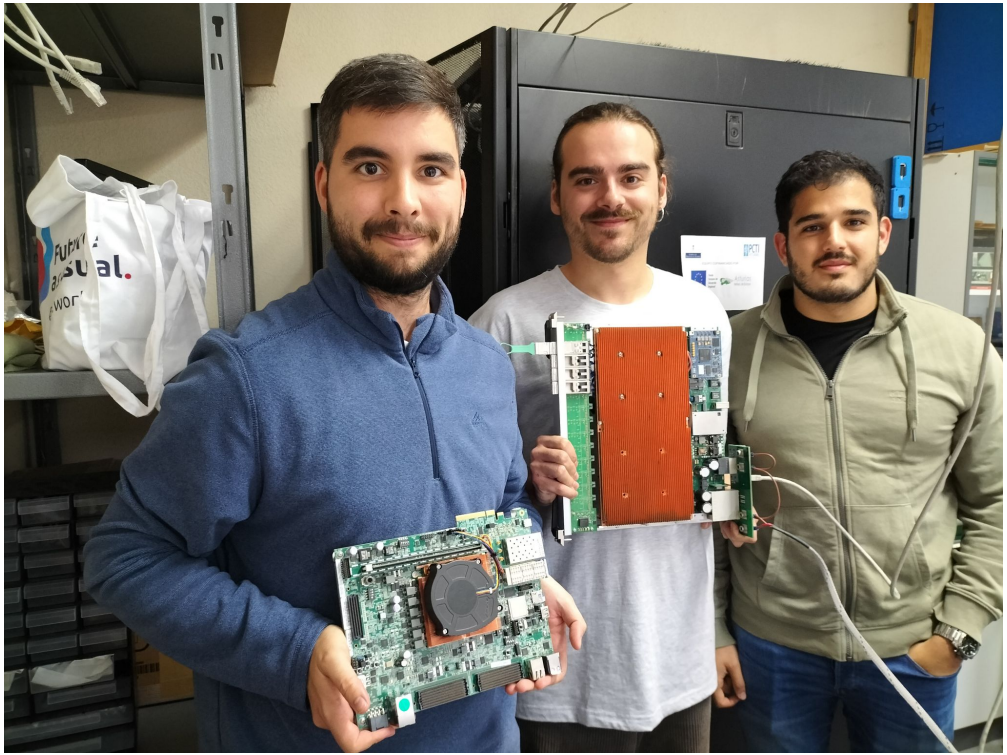




The end

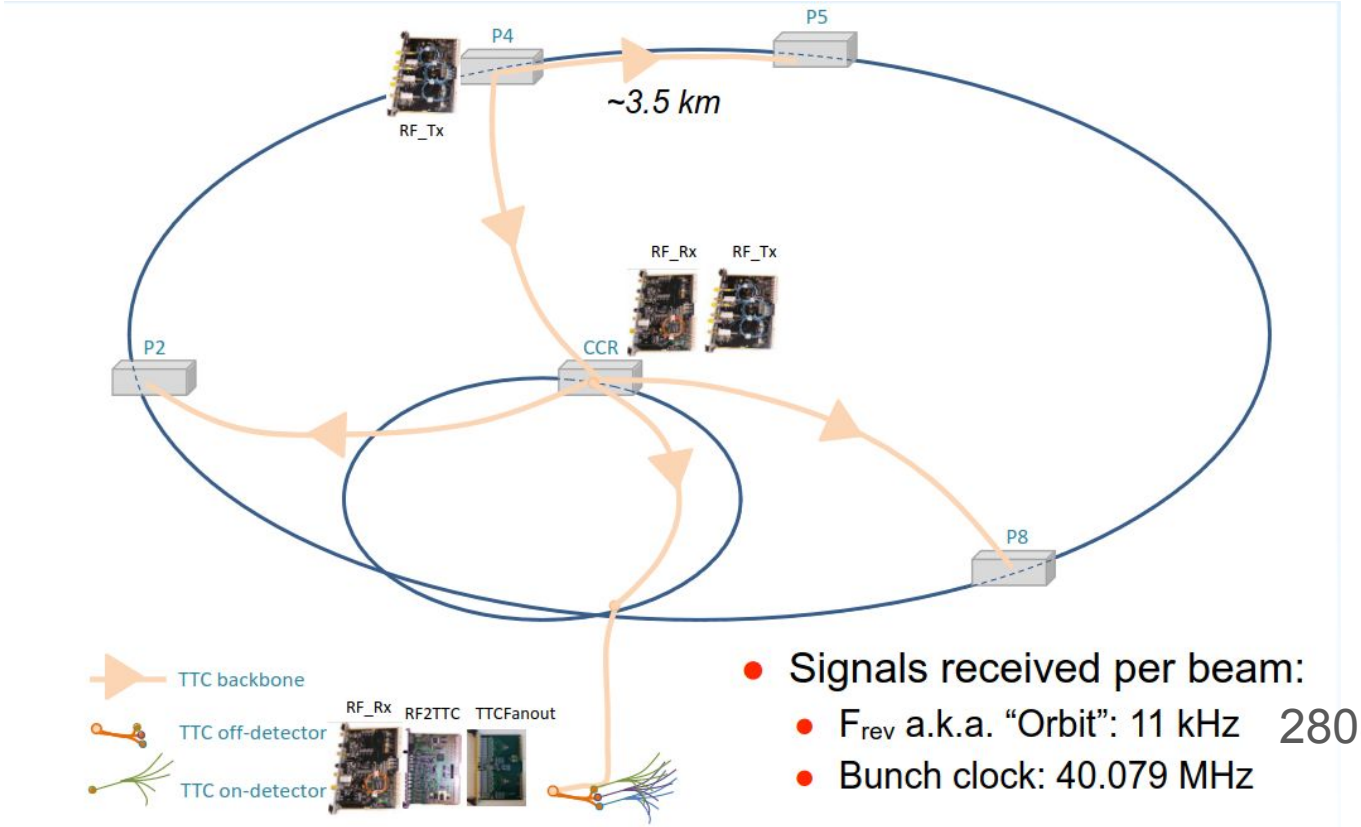
Thank you for your time!

Questions?



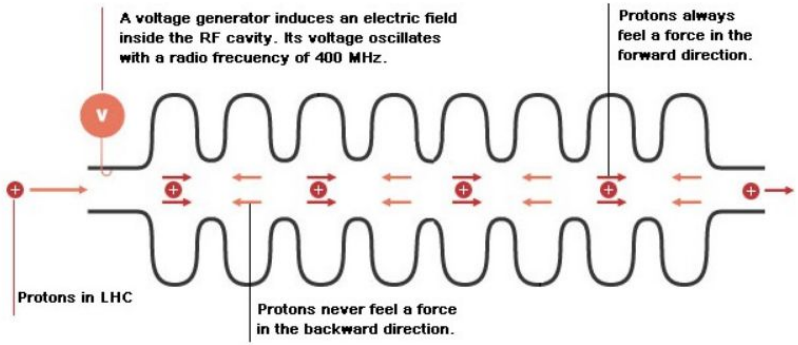
Back up

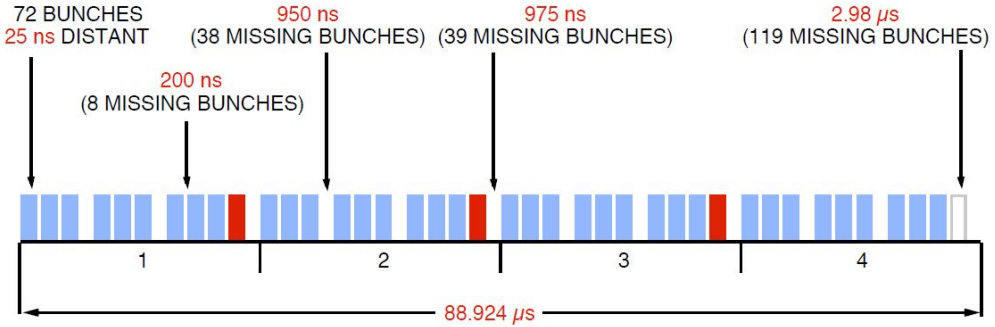
Backup slides



- Signals received per beam:
  - F_{rev} a.k.a. “Orbit”: 11 kHz
  - Bunch clock: 40.079 MHz

2808 b



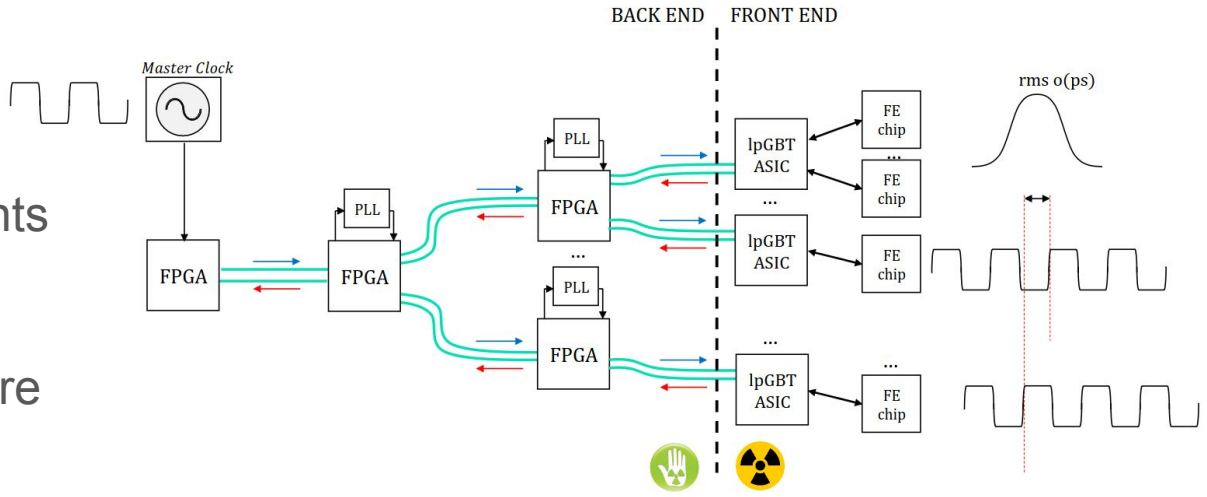


In order to maintain an acceptable filling factor in the LHC with the 72-bunch PS trains, the SPS batches which will be injected into the LHC will comprise groups of 3, 3 and then 4 PS trains.

As a result of this change the number of bunch crossings per orbit will be reduced from 2835 to 2808. Note that this applies only to ATLAS and CMS.

Timing in LHC - Cleaning

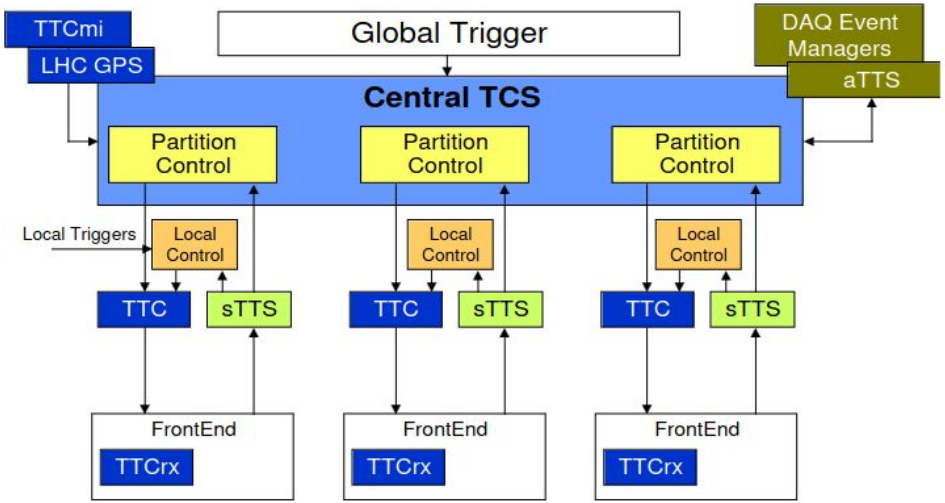
- Signal stability requirements over +1000 end points.
- Long-term environmental variations such temperature can affect clock phase.
- Fast variations can be cleaned at the last PLL of the backend FPGA chain.



TCLink

A Timing Compensated High-Speed Optical Link for the HL-LHC experiments

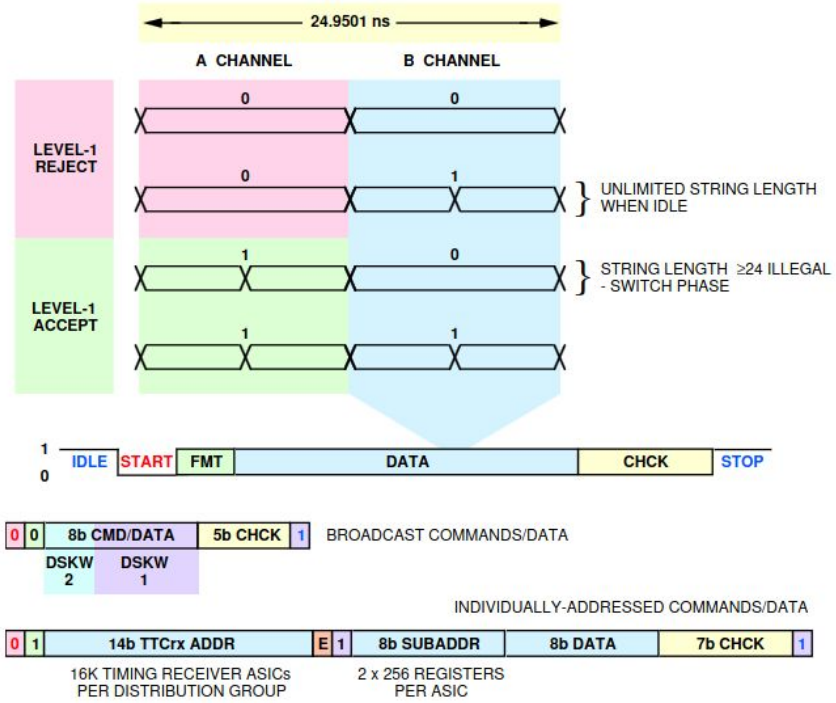
TCS



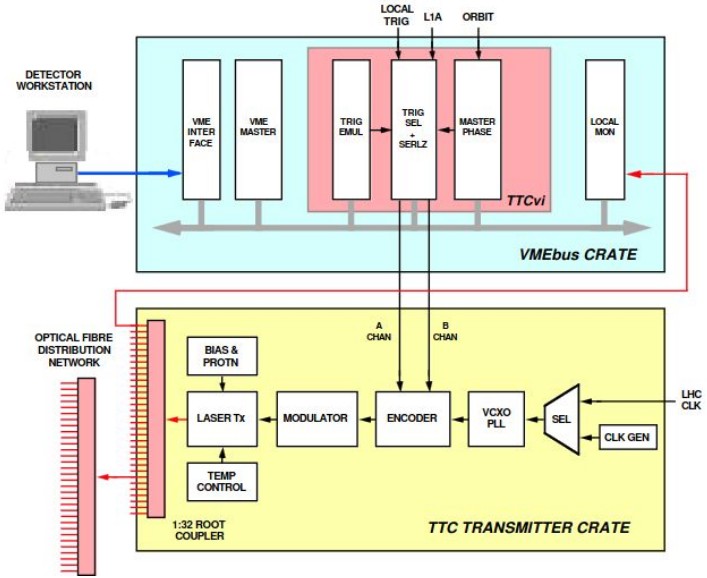
- The main task of the L1 Trigger Control System (TCS) is to control the delivery of L1 Trigger Accepts(L1A) generated by the Global Trigger, depending on the status of the readout electronics and the data acquisition.

- This status is derived from local state machines that emulate the front-end buffers occupation, as well as from direct information transmitted back by the CMS subsystems through the Trigger Throttling System (TTS).
- TCS is also responsible for generating synchronization and fast reset commands, as well as to control the delivery of test and calibration triggers.
- TCS uses the TTC network to distribute information to the subsystems.

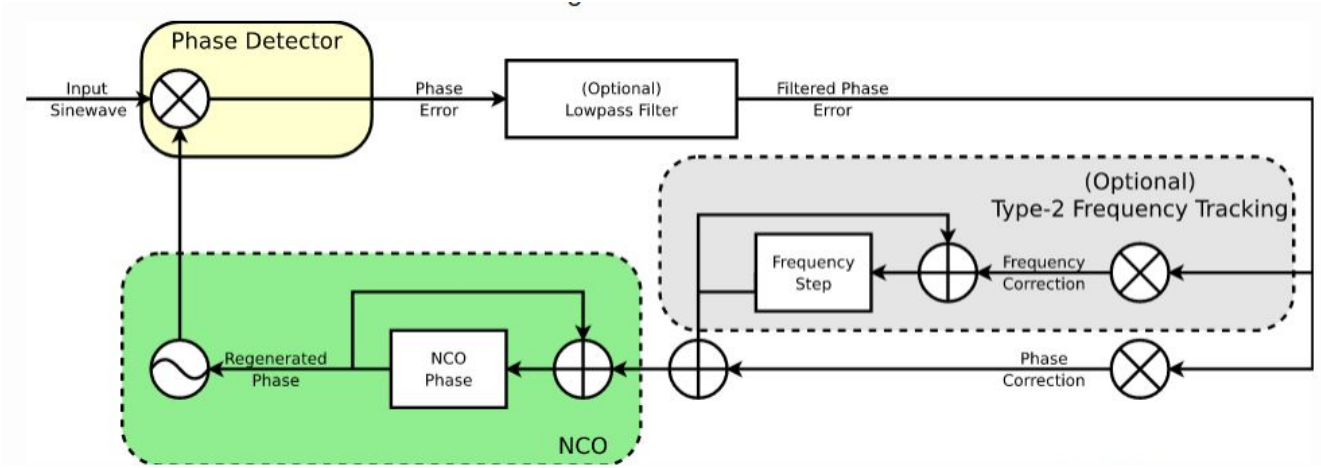
TTC Encoding



- Two data channels are time-division multiplexed (TDM) and encoded biphase mark at 160.32 MBaud (four times the LHC bunch-crossing rate). This is sufficiently close to the standard Sonet OC-3 (CCITT SDH STM-1) rate of 155.52 MBaud.



PLL



- The loop begins with an incoming sine wave that is passed into a phase detector. The phase detector is used to compare the phase of the incoming sine wave against a reconstructed sine wave produced internally. The output of this phase detector is an error signal. This error signal is then optionally filtered, and fed into two portions of the circuit: one to track frequency and the other to track phase. These two portions combine within a Numerically Controlled Oscillator (NCO) to create a new phase for the reconstructed sine wave. That phase is then used as an input to a sine wave generator to create a reconstructed sine wave, which is then used as the second input to the phase detector and the loop repeats.